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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,899	07/28/2003	Yi-Nan Chen	10112531	7431

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EXAMINER

VU, DAVID

ART UNIT PAPER NUMBER

2818

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/628,899

Applicant(s)

CHEN ET AL.

Examiner

DAVID VU

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06/27/05.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) 6 and 19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-18 and 20-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 1, 4, 5, 7 and 10-12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster et al. (US 6,455,369, herein after Forster) in view of Kudelka (US Pat. 6,566,273)

Regarding claims 1, 4, 5, 7 and 10, Forster discloses in figs. 3A-4O a method for fabricating a bottle-shaped trench capacitor, comprising the steps of: forming a trench in a substrate (fig. 3A); filling a lower portion of the trench with a first conductive layer S5

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surrounded by a doped layer S4 (fig. 3E); forming a conformable insulating layer {(S6 of fig G) or (S31 of fig. 3I)} overlying the substrate and an inner surface of the upper portion of the trench to cover the first conductive layer S5 and the doped layer S4 (fig. 3F); performing a heat treatment on the substrate to form a doping region S7 (fig. 3G) in the substrate near the doped layer S4 to serve as a buried bottom plate (col. 12, lines 5-8); anisotropically etching the insulating layer to form a collar insulating layer over a sidewall of an upper portion of the trench (col. 10, lines 3-4); removing the first conductive layer and the doped layer using the collar insulating layer as a mask to expose the surface of the doping region (fig. 3H); etching a portion of the exposed doping region to form a bottle-shaped trench (col. 12, lines 19-21 and fig. 3I); forming a conformable rugged polysilicon layer S8 (col. 12, lines 21-24 and fig. 3J) and a conformable capacitor dielectric layer S10 in the lower portion of the trench; and filling the lower portion of the trench with a second conductive layer S11 to serve as a top plate (col. 10, lines 36-41 and col. 12, lines 43-46).

Forster fails to disclose using HF vapor as an etching agent. However, Kudelka teaches the doped layer (ASG/TEOS 105) (col. 4, lines 31-41 and figs. 5-7) is removed by HF vapor (col. 4, line 62 through col. 5, line 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Forster by using the HF vapor as an etching agent as taught by Kudelka since the HF vapor is a well known material for an etching processes. The etching agent is material dependent. One of the ordinary skilled in the art would have been motivated to select a desired etching agent for the material to be selectively etched.

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Regarding claim 11, Forster discloses the capacitor dielectric layer comprises a silicon nitride layer (col. 10, lines 36-38 and col. 12, lines 43-44).

Regarding claim 12, Forster discloses performing a gas phase doping (GPD) after the rugged polysilicon layer is formed (col. 10, lines 13-21).

2. Claims 2, 3, 13, 14, 18, 20, 23 and 24 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster (US 6,455,369) in view of Kudelka (US Pat. 6,566,273) and further in view of Chidambarao et al. (US Pat. 6,707,095, herein after Chidambarao).

Regarding claims 2, 3, 13, 14, 18 and 20, Forster discloses in figs. 3A-4O a method for fabricating a bottle-shaped trench capacitor, comprising the steps of: providing a substrate covered by a masking layer having an opening therein; etching the substrate under the opening to form a trench therein (fig. 3A); filling a lower portion of the trench with a first conductive layer S5 surrounded by a doped layer S4 (fig. 3E); forming a conformable insulating layer {(S6 of fig G) or (S31 of fig. 3I)} overlying the substrate and an inner surface of the upper portion of the trench to cover the first conductive layer S5 and the doped layer S4 (fig. 3F); performing a heat treatment on the substrate to form a doping region S7 (fig. 3G) in the substrate near the doped layer S4 to serve as a buried bottom plate (col. 12, lines 5-8); anisotropically etching the insulating layer to form a collar insulating layer over a sidewall of an upper portion of the trench (col. 10, lines 3-4); removing the first conductive layer and the doped layer using the collar insulating layer as a mask to expose the surface of the doping region (fig. 3H); etching a portion of the exposed doping region to form a bottle-shaped trench (col. 12,

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lines 19-21 and fig. 3I); forming a conformable rugged polysilicon layer S8 (col. 12, lines 21-24 and fig. 3J) and a conformable capacitor dielectric layer S10 in the lower portion of the trench; and filling the lower portion of the trench with a second conductive layer S11 to serve as a top plate (col. 10, lines 36-41 and col. 12, lines 43-46).

Forster fails to disclose forming the first/second wiring layers after forming the trench capacitor. However, Chidambarrao discloses in fig. 19, col. 13, lines 20-22 and col. 16, lines 52-53 a gate conductor (GC) and a wordline 32 is formed on the trench capacitor. It would have been obvious to one with ordinary skill in the art at the time of the invention to use a gate conductor (GC) and a wordline as taught by Chidambarrao in the process of Forster. As recognized by one skilled in the art, the gate conductor (GC) and the wordline is defined the channel of the MOSFET and served as a wiring layer.

Forster also fails to disclose using HF vapor as an etching agent. However, Kudelka teaches the doped layer (ASG/TEOS 105) (col. 4, lines 31-41 and figs. 5-7) is removed by HF vapor (col. 4, line 62 through col. 5, line 17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Forster by using the HF vapor as an etching agent as taught by Kudelka since the HF vapor is a well known material for an etching processes. The etching agent is material dependent. One of the ordinary skilled in the art would have been motivated to select a desired etching agent for the material to be selectively etched.

Regarding claim 23, Forster discloses the capacitor dielectric layer comprises a silicon nitride layer (col. 10, lines 36-38 and col. 12, lines 43-44).

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Regarding claim 24, Forster discloses performing a gas phase doping (GPD) after the rugged polysilicon layer is formed (col. 10, lines 13-21).

3. Claim 8 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster (US 6,455,369) in view of Kudelka (US Pat. 6,566,273) and further in view of Bronner et al. (US Pat. 6,177,696, herein after Bronner).

Forster fails to disclose the heat treatment is performed at about 900 to 1100°C. However, Bronner teaches in col. 5, lines 29-41 that the buried plate 14 is formed at a temperature of 1050°C. It would have been obvious to one with ordinary skill in the art at the time of the invention to use the heat treatment as taught by Bronner in the process of Forster. The heat treatment temperature does not define patentable over Forster in view of Bronner since the temperature is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific temperature does not provide any critical or unexpected results to the method of manufacturing a trench capacitor. Rather, it is merely an obvious selection of the heat treatment temperature based on desired functional characteristics determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

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4. Claim 9 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster (US 6,455,369) in view of Kudelka (US Pat. 6,566,273) and further in view of Schrems (US Pat. 6,580,110)

Forster discloses wet etching but fails to disclose the wet chemical is BHF or  $\text{NH}_4\text{OH}$ . However, Schrems teaches the wet etching such as  $\text{NH}_4\text{OH}$  or HF is used for widening the lower region of the trench (col. 11, lines 33-35 and col. 12, lines 42-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Forster by using the etching agent as taught by Schrems since the wet chemical such as BHF or  $\text{NH}_4\text{OH}$  is a well known etching agent for a wet etching processes. The wet etching agent is material dependent. One of the ordinary skilled in the art would have been motivated to select a desired wet etching agent for the material to be selectively etched.

5. Claim 21 is rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster (US 6,455,369) in view of Kudelka (US Pat. 6,566,273); in view of Chidambarao (US Pat. 6,707,095) and further in view of Bronner (US Pat. 6,177,696).

Forster fails to disclose the heat treatment is performed at about 900 to 1100°C. However, Bronner teaches in col. 5, lines 29-41 that the buried plate 14 is formed at a temperature of 1050°C. It would have been obvious to one with ordinary skill in the art at the time of the invention to use the heat treatment as taught by Bronner in the process of Forster. The heat treatment temperature does not define patentable over Forster in view of Bronner since the temperature is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific



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temperature does not provide any critical or unexpected results to the method of manufacturing a trench capacitor. Rather, it is merely an obvious selection of the heat treatment temperature based on desired functional characteristics determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

6. Claims 16 and 22 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster (US 6,455,369) in view of Kudelka (US Pat. 6,566,273); in view of Chidambarao (US Pat. 6,707,095) and further in view of Schrems (US Pat. 6,580,110).

Forster discloses wet etching but fails to disclose the wet chemical is BHF or  $\text{NH}_4\text{OH}$ . However, Schrems teaches the wet etching such as  $\text{NH}_4\text{OH}$  or HF is used for widening the lower region of the trench (col. 11, lines 33-35 and col. 12, lines 42-47). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Forster by using the etching agent as taught by Schrems since the wet chemical such as BHF or  $\text{NH}_4\text{OH}$  is a well known etching agent for a wet etching processes. The wet etching agent is material dependent. One of the ordinary skilled in the art would have been motivated to select a desired wet etching agent for the material to be selectively etched.

7. Claims 15 and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Forster (US 6,455,369) in view of Kudelka (US Pat. 6,566,273); in view of Chidambarao

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(US Pat. 6,707,095) and further in view of Mandelman et al. (US Pat. 6,437,401, herein after Mandelman).

Forster fails to disclose the step of forming a recess. However, Mandelman teaches the steps of isotropically etching the pad oxide layer 9 to form a recess with a depth of about 2-20nm (col. 7, lines 6); and filling the recess with silicon nitride 14 (col. 8, lines 4-16 and fig. 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Forster and Chidambarrao by using a recess as taught by Mandelman since the nitride layer is formed under the recess will serve as an etch barrier during a subsequent silicon etch which is used to form a collar insulating layer over a sidewall of an upper portion of the trench. The specific depth of the recess does not provide any critical or unexpected results to the method of manufacturing a trench capacitor. Rather, it is merely an obvious selection of the depth of the recess based on desired functional characteristics determinable by routine experimentation. In *Aller*, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In *re Aller*, 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995).

## Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If

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attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Vu

July 07, 2005.